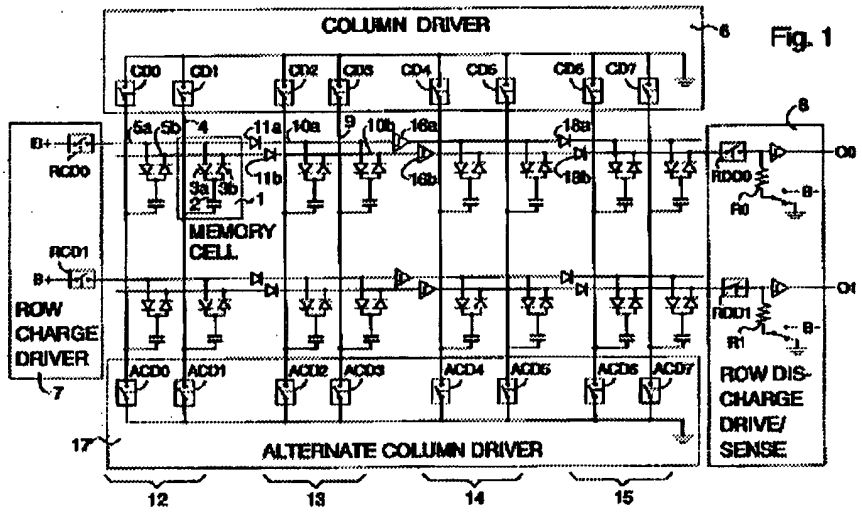

Fig. 1

United States Patent [19]
Harshfield

[11] **Patent Number: 5,818,749**
[45] **Date of Patent: Oct. 6, 1998**

[54] **INTEGRATED CIRCUIT MEMORY DEVICE**

[75] Inventor: **Steven T. Harshfield**, Emmett, Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **884,864**

[22] Filed: **Feb. 24, 1997**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 848,647, Dec. 1, 1994, Pat. No. 5,646,879, which is a continuation of Ser. No. 110,226, Aug. 20, 1993, Pat. No. 5,379,250.

[51] Int. Cl.[6] G11C 17/08

[52] U.S. Cl. 365/105; 365/96; 365/175; 365/225.7

[58] Field of Search 365/105, 96, 175, 365/225.7; 257/526, 530

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Primary Examiner—Son T. Dinh
Attorney, Agent, or Firm—Fletcher, Yoder & Edwards

[57] **ABSTRACT**

A memory array using structure changing memory elements in a reverse biased diode array is disclosed. A memory cell is programmed and read by reverse biasing the diode to overcome the diode's breakdown voltage. The disclosed reversed biased diode array exhibits much less substrate current leakage than a similar forward biased diode array.

47 Claims, 8 Drawing Sheets

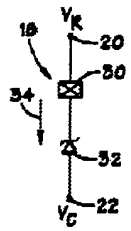


Fig 3

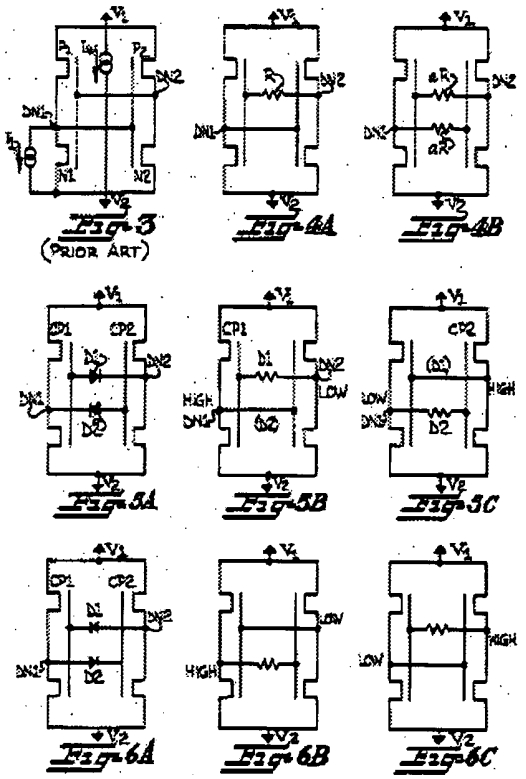


Fig. 3 (PRIOR ART)

Fig. 4A

Fig. 4B

Fig. 5A

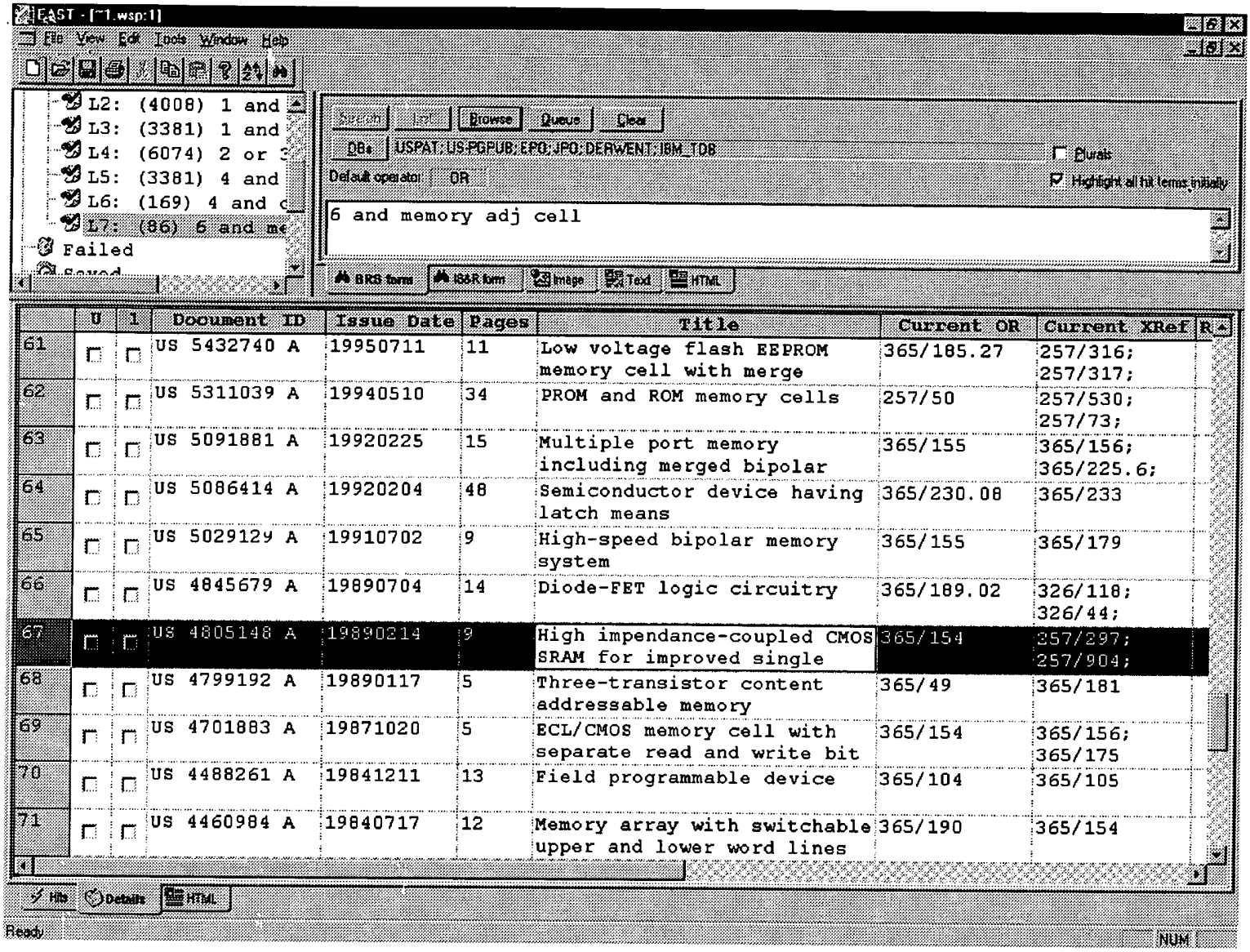
Fig. 5B

Fig. 5C

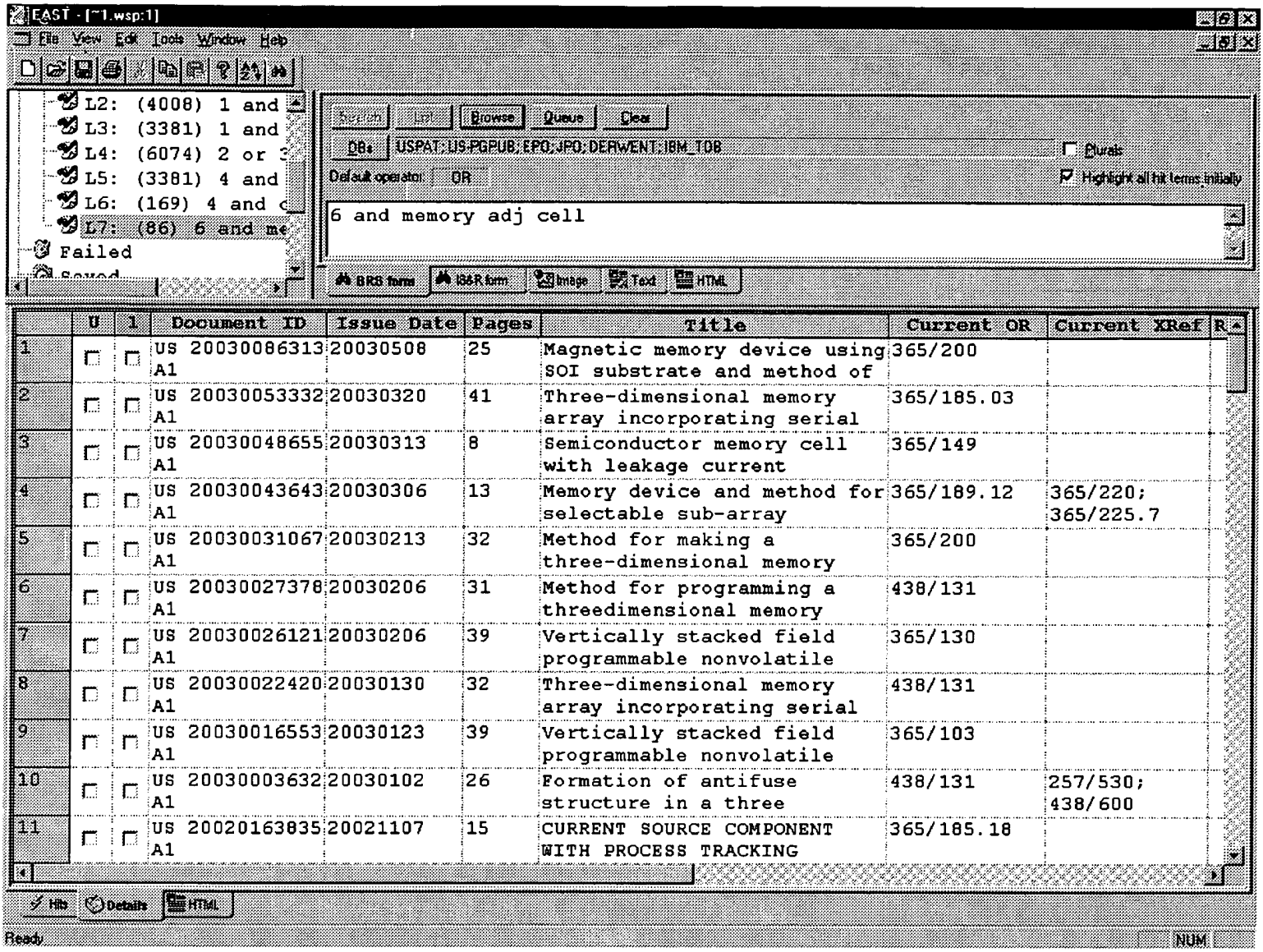
Fig. 6A

Fig. 6B

Fig. 6C



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
61	☐	☐	US 5432740 A	19950711	11	Low voltage flash EEPROM memory cell with merge	365/185.27	257/316; 257/317;	
62	☐	☐	US 5311039 A	19940510	34	PROM and ROM memory cells	257/50	257/530; 257/73;	
63	☐	☐	US 5091881 A	19920225	15	Multiple port memory including merged bipolar	365/155	365/156; 365/225.6;	
64	☐	☐	US 5086414 A	19920204	48	Semiconductor device having latch means	365/230.08	365/233	
65	☐	☐	US 5029129 A	19910702	9	High-speed bipolar memory system	365/155	365/179	
66	☐	☐	US 4845679 A	19890704	14	Diode-FET logic circuitry	365/189.02	326/118; 326/44;	
67	☐	☐	US 4805148 A	19890214	9	High impendance-coupled CMOS SRAM for improved single	365/154	257/297; 257/904;	
68	☐	☐	US 4799192 A	19890117	5	Three-transistor content addressable memory	365/49	365/181	
69	☐	☐	US 4701883 A	19871020	5	ECL/CMOS memory cell with separate read and write bit	365/154	365/156; 365/175	
70	☐	☐	US 4488261 A	19841211	13	Field programmable device	365/104	365/105	
71	☐	☐	US 4460984 A	19840717	12	Memory array with switchable upper and lower word lines	365/190	365/154	



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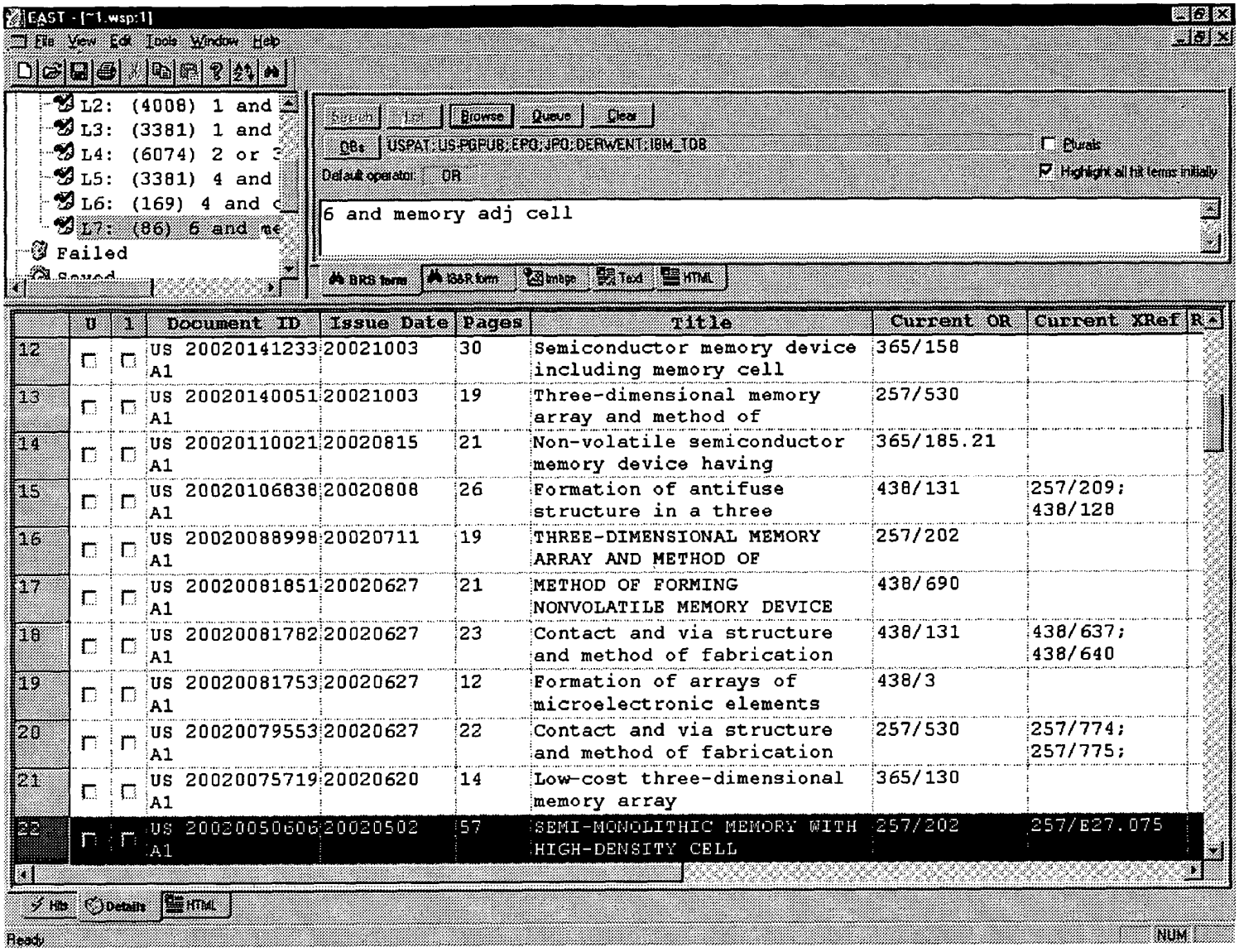
1	☐	☐	US 20030086313 A1	20030508	25	Magnetic memory device using SOI substrate and method of	365/200		
2	☐	☐	US 20030053332 A1	20030320	41	Three-dimensional memory array incorporating serial	365/185.03		
3	☐	☐	US 20030048655 A1	20030313	8	Semiconductor memory cell with leakage current	365/149		
4	☐	☐	US 20030043643 A1	20030306	13	Memory device and method for selectable sub-array	365/189.12	365/220; 365/225.7	
5	☐	☐	US 20030031067 A1	20030213	32	Method for making a three-dimensional memory	365/200		
6	☐	☐	US 20030027378 A1	20030206	31	Method for programming a threedimensional memory	438/131		
7	☐	☐	US 20030026121 A1	20030206	39	Vertically stacked field programmable nonvolatile	365/130		
8	☐	☐	US 20030022420 A1	20030130	32	Three-dimensional memory array incorporating serial	438/131		
9	☐	☐	US 20030016553 A1	20030123	39	Vertically stacked field programmable nonvolatile	365/103		
10	☐	☐	US 20030003632 A1	20030102	26	Formation of antifuse structure in a three	438/131	257/530; 438/600	
11	☐	☐	US 20020163835 A1	20021107	15	CURRENT SOURCE COMPONENT WITH PROCESS TRACKING	365/185.18		



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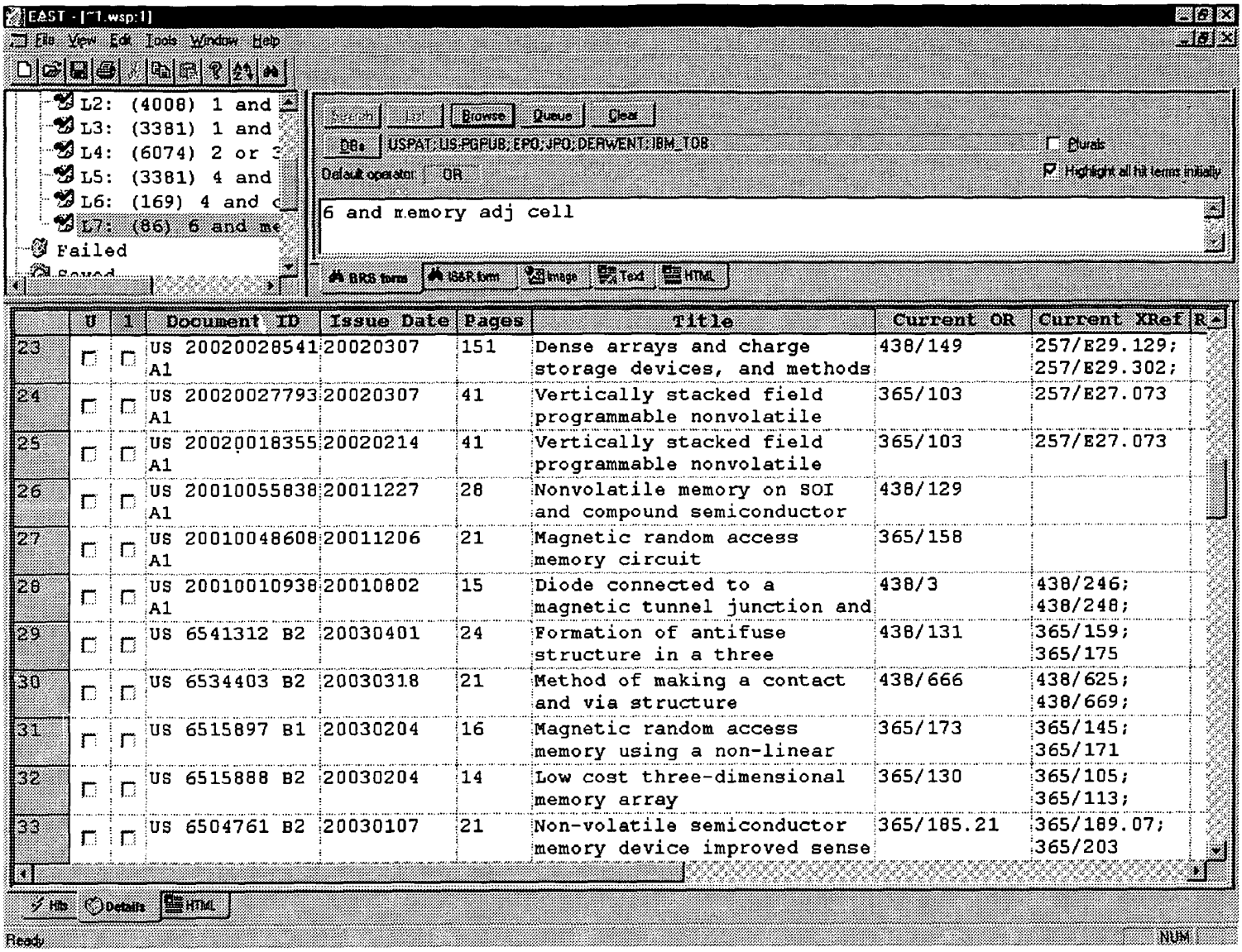
12	☐	☐	US 20020141233 A1	20021003	30	Semiconductor memory device including memory cell	365/158		
13	☐	☐	US 20020140051 A1	20021003	19	Three-dimensional memory array and method of	257/530		
14	☐	☐	US 20020110021 A1	20020815	21	Non-volatile semiconductor memory device having	365/185.21		
15	☐	☐	US 20020106838 A1	20020808	26	Formation of antifuse structure in a three	438/131	257/209; 438/128	
16	☐	☐	US 20020088998 A1	20020711	19	THREE-DIMENSIONAL MEMORY ARRAY AND METHOD OF	257/202		
17	☐	☐	US 20020081851 A1	20020627	21	METHOD OF FORMING NONVOLATILE MEMORY DEVICE	438/690		
18	☐	☐	US 20020081782 A1	20020627	23	Contact and via structure and method of fabrication	438/131	438/637; 438/640	
19	☐	☐	US 20020081753 A1	20020627	12	Formation of arrays of microelectronic elements	438/3		
20	☐	☐	US 20020079553 A1	20020627	22	Contact and via structure and method of fabrication	257/530	257/774; 257/775;	
21	☐	☐	US 20020075719 A1	20020620	14	Low-cost three-dimensional memory array	365/130		
22	☐	☐	US 20020050606 A1	20020502	57	SEMI-MONOLITHIC MEMORY WITH HIGH-DENSITY CELL	257/202	257/E27.075	



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23	☐	☐	US 20020028541 A1	20020307	151	Dense arrays and charge storage devices, and methods	438/149	257/E29.129; 257/E29.302;	
24	☐	☐	US 20020027793 A1	20020307	41	Vertically stacked field programmable nonvolatile	365/103	257/E27.073	
25	☐	☐	US 20020018355 A1	20020214	41	Vertically stacked field programmable nonvolatile	365/103	257/E27.073	
26	☐	☐	US 20010055838 A1	20011227	28	Nonvolatile memory on SOI and compound semiconductor	438/129		
27	☐	☐	US 20010048608 A1	20011206	21	Magnetic random access memory circuit	365/158		
28	☐	☐	US 20010010938 A1	20010802	15	Diode connected to a magnetic tunnel junction and	438/3	438/246; 438/248;	
29	☐	☐	US 6541312 B2	20030401	24	Formation of antifuse structure in a three	438/131	365/159; 365/175	
30	☐	☐	US 6534403 B2	20030318	21	Method of making a contact and via structure	438/666	438/625; 438/669;	
31	☐	☐	US 6515897 B1	20030204	16	Magnetic random access memory using a non-linear	365/173	365/145; 365/171	
32	☐	☐	US 6515888 B2	20030204	14	Low cost three-dimensional memory array	365/130	365/105; 365/113;	
33	☐	☐	US 6504761 B2	20030107	21	Non-volatile semiconductor memory device improved sense	365/185.21	365/189.07; 365/203	